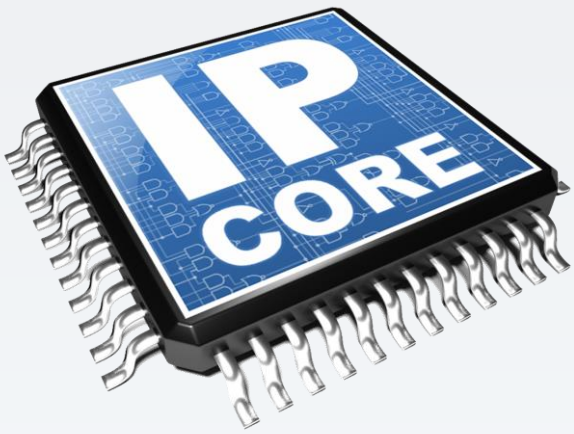
SpaceWire Router IP Core

The SpaceWire Router IP core is a macrocell offering a configurable and flexible solution for high data-rate routing switch functionality for on-board satellite networking. It is based on the SpaceWire protocol, defining bi-directional, full-duplex, serial data communication link, and it is compliant with the SpaceWire standard ECSS-E-ST-50-12C Rev.1 (SpaceWire Routing Switch specification).

The SpaceWire Router IP Core features a parametrized number of SpaceWire ports, based on proprietary SpaceWire CODEC IP Core, and host-side data ports, based on asynchronous FIFO interfaces. The host data ports can be optionally equipped with AMBA AXI interface. The SpaceWire Router IP core has been validated and prototyped in ESA project.

Key Features

- Compliant with ECSS-E-ST-50-12C Rev.1 standard
- Highly customisable to fulfil user needs
- Up to 31 SpW and/or host data (FIFO) ports
- Path addressing, logical addressing, regional addressing and multicast addressing support
- SpW TX bit rate and link start mode programmability for each available SpW port
- Host data ports with simple FIFO-based interface
- Time-Code distribution support in both slave and master mode
- SpW links configuration/check and port addresses mapping/check via SpW packets
- Optional support to RMAP target commands in conformance with ECSS-E-ST-50-52C standard
- Optional support to AMBA AXI-4 Memory Mapped interfaces, backward compatible with AXI-3 specification
- Technology-independent, VHDL IP core, successfully implemented and tested on many FPGA devices for space



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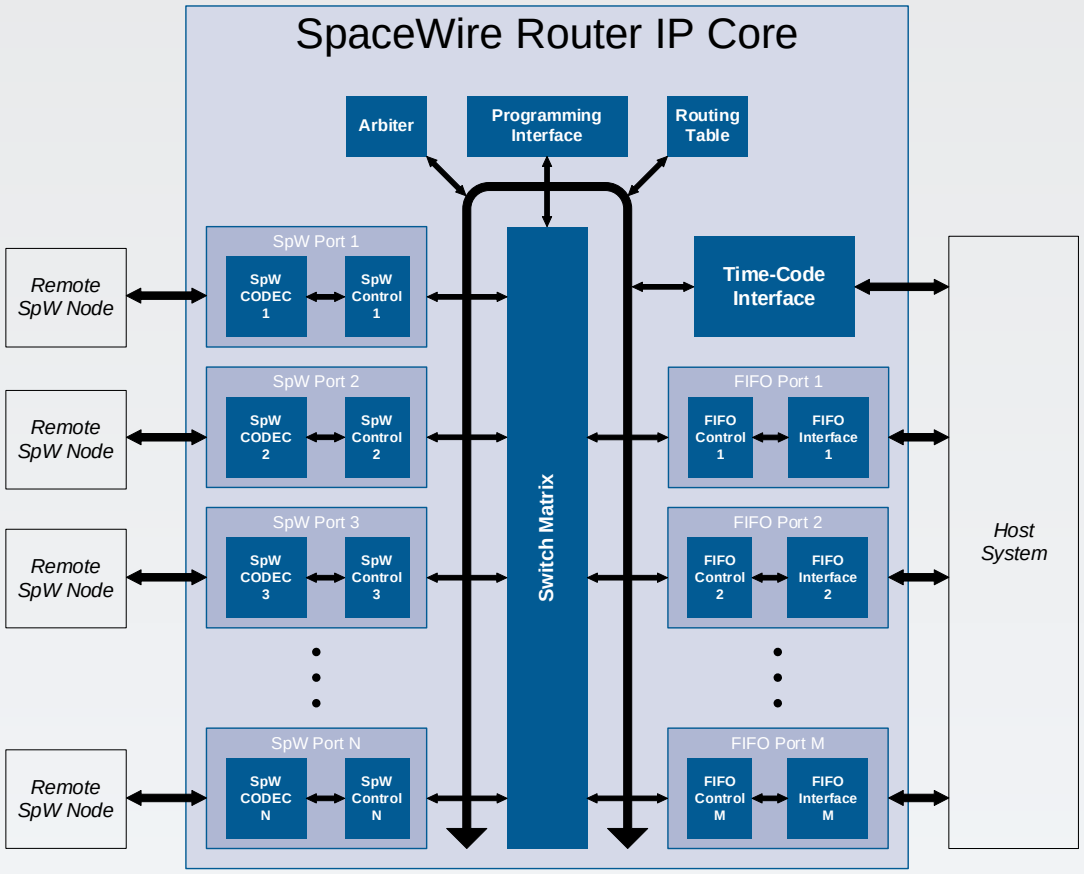
Architectural features

Besides the parametrized number of SpaceWire ports and host data (FIFO) ports, the architecture features the following units: switch matrix, fully programmable routing table, arbiter logic, programming interface and time-code host interface.

The SpaceWire port units and the host data port units offer data connectivity between nodes. The switch matrix, with router table and arbiter, dynamically connect the input nodes with the appropriate output nodes, relying on packet addressing. The programming interface allows SpaceWire links configuration/check and logical/regional/multicast addresses mapping. RMAP target commands also can be supported by employing optional hardware decoder in conformance with ECSS-E-ST-50-52C standard (SpaceWire RMAP Target specification). The time-code interface offers support to both slave and master modes, with time-codes distribution throughout the network: the time-codes received by the router on any port are checked and forwarded to all the other network nodes.



Synthesis results*

Microchip RTAX2000S FPGA

Configuration	Comb	Comb%	Reg	Reg%	RAM blocks	RAM %
4 SpW ports + 1 host port	6575	30.576%	4378	40.718%	10	15.625%
8 SpW ports + 1 host port	11203	52.097%	6817	63.402%	18	28.125%

* Hardware resource occupation and performance figures can be requested for the specific target device

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