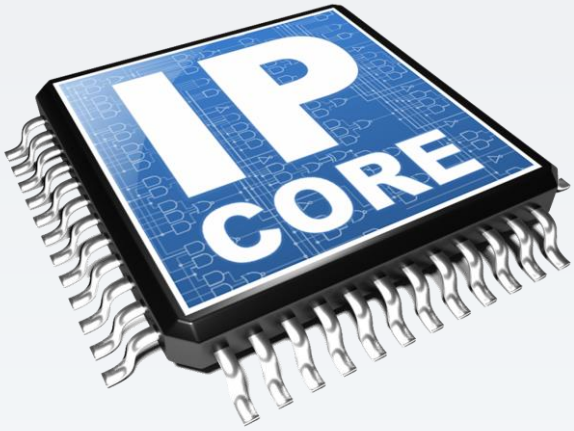
SpaceWire CODEC IP Core

The SpaceWire CODEC IP core is a very compact macrocell providing a complete and configurable interfacing solution for high data-rate communications compliant with the standard ECSS-E-ST-50-12C. The SpaceWire protocol defines a bi-directional, full-duplex, serial data communication link, and it is based on LVDS physical layer, resulting in a low-power high-speed link. The SpaceWire CODEC IP core has been tested at multiple levels, it is interoperable with other SpaceWire commercial products (e.g., conformance testers), it has been validated in ESA space project, and it has been integrated in space flight hardware for Earth observation missions (e.g., ESA Sentinel-3 mission)

Key Features

- ECSS-E-ST-50-12C compliant (encoder-decoder specification)
- Highly customisable to fulfil user needs
- SpaceWire TX data-rate and link start mode programmability
- Simple FIFO-based host interface or AMBA AXI bus interface (on request)
- Time-code transmission and reception support
- Configuration and status/error interface
- Fault tolerant IP with EDAC FIFOs (on request)
- Optional RMAP target with dedicated hardware decoder
- Low power, low complexity, high frequency



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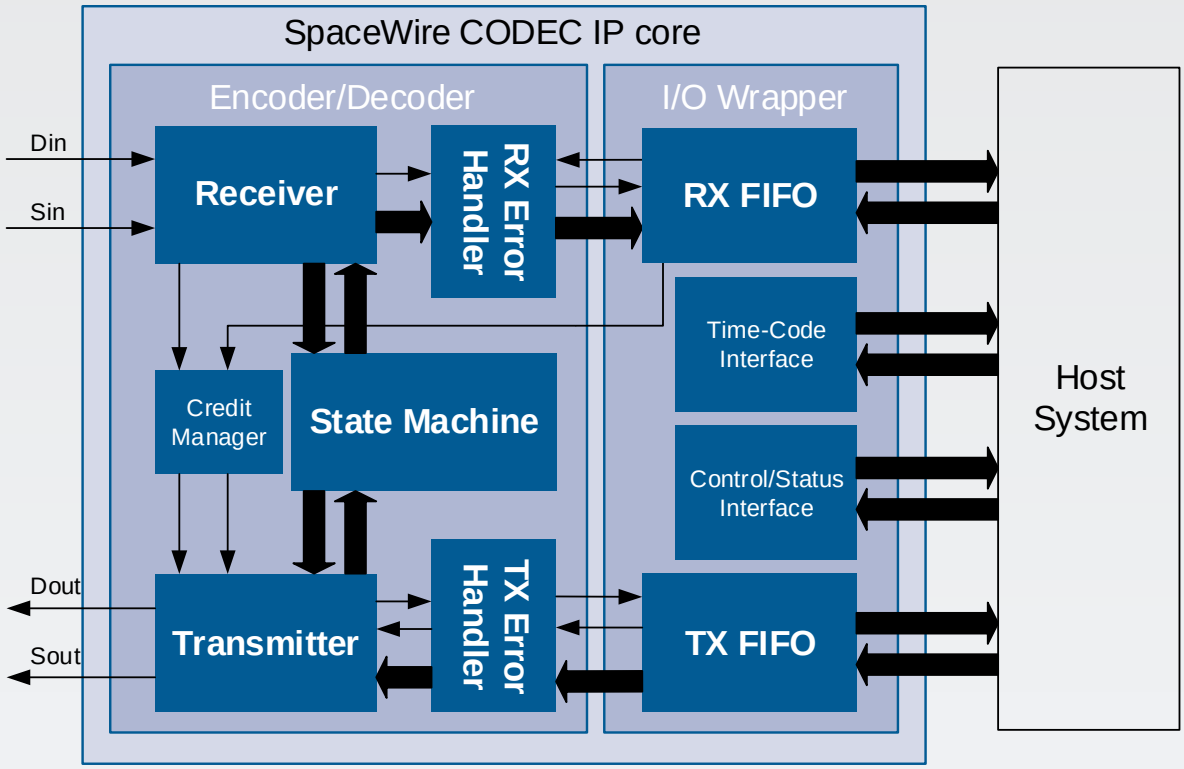
Architectural features

The SpaceWire CODEC IP core is composed of: the encoder-decoder unit and the I/O wrapper unit. The encoder-decoder unit implements the SpaceWire protocol logic, with transmitter and receiver chains and with state machine logic as defined within the standard. Some dedicated circuitry is used to safely handle the asynchronous clock domain obtained from the received data (i.e., SpaceWire receiver clock) and to manage the clock domain crossing.

The I/O wrapper unit offers a simple data interface with host system based on TX and RX FIFOs with (i.e., buffers with depth of 64 characters and width of 9 bits). This host data interface can be optionally equipped (on request) with an AMBA AXI interface. The I/O wrapper unit also implements the host configuration and status/error interface for a correct management of the operating mode and the SpaceWire link.



Synthesis results on Microsemi RTAX2000S FPGA

	Combinational	Registers	RAM blocks
TX/RX FIFOs with FFs	5.62 % (1208/21504)	15.41 % (1657/10752)	0.0 % (0/64)
TX/RX FIFOs with RAMs	2.97 % (639/21504)	3.53 % (380/10752)	3.125 % (2/64)
TX/RX FIFOs with EDAC RAMs	3.51 % (754/21504)	3.85 % (414/10752)	3.125 % (2/64)

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