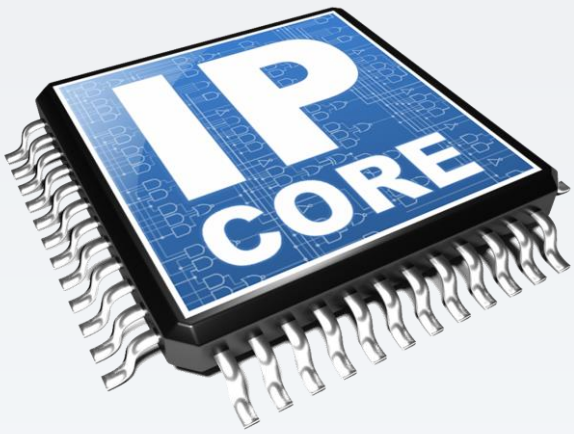
# SpaceWire CODEC IP Core

The SpaceWire CODEC IP core is a very compact macrocell providing a complete and configurable interfacing solution for high data-rate communications compliant with the SpaceWire standard ECSS-E-ST-50-12C Rev.1. The SpaceWire protocol defines a bi-directional, full-duplex, serial data communication link, and it is based on LVDS physical layer, resulting in a low-power high-speed link. The SpaceWire CODEC IP core has been tested at multiple levels, it is interoperable with other SpaceWire commercial products (e.g., conformance testers), it has been validated in ESA space project, and it has been **integrated in space flight hardware for Earth observation missions** (e.g., **ESA Sentinel-3 mission**, **ESA Euclid mission**) and others (e.g., **Iridium NEXT constellation**)

## Key Features

- Compliant with ECSS-E-ST-50-12C Rev.1 standard (SpaceWire Encoder-Decoder specification)
- Highly customisable to fulfil user needs
- SpW TX bit rate and link start mode programmability
- Simple FIFO-based host data interface
- Optional support to AMBA AXI bus interface with DMA functionality
- Time-Code support for transmission and reception, with automatic validity check of received time-codes
- Control/configuration and status/error dedicated host interface
- Fault tolerant IP with configurable EDAC FIFOs
- Optional support to RMAP Target commands in conformance with ECSS-E-ST-50-52C standard (SpaceWire RMAP Target specification)
- Technology-independent, VHDL IP core, successfully implemented and tested on many FPGA devices for space

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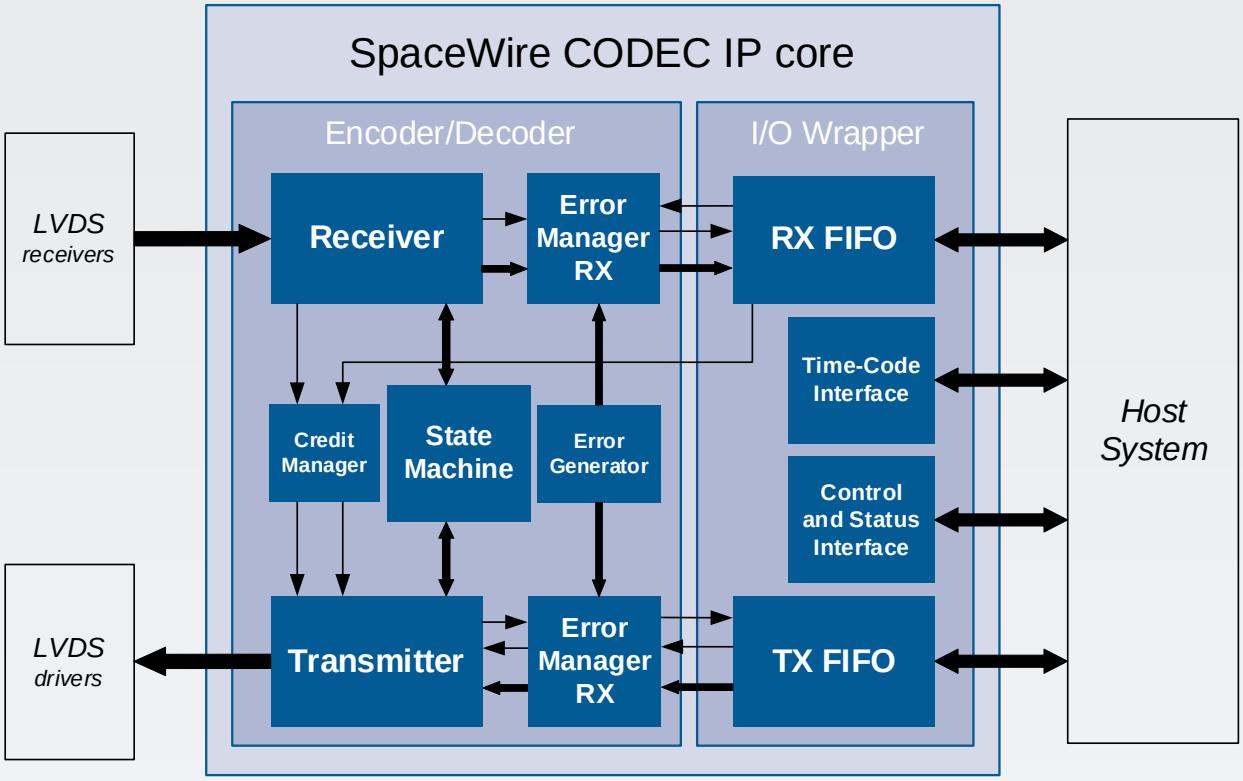
# Architectural features

The SpaceWire CODEC IP core is composed of: the encoder-decoder unit and the I/O wrapper unit. The encoder-decoder unit implements the SpaceWire protocol logic, with transmitter and receiver chains and with state machine logic as defined within the standard. Some dedicated circuitry is used to safely handle the asynchronous clock domain obtained from the received data (i.e., SpaceWire receiver clock) and to manage the clock domain crossing.

The I/O wrapper unit offers a simple data interface with host system based on TX and RX FIFOs with (i.e., buffers with depth of 64 characters and width of 9 bits). This host data interface can be optionally equipped (on request) with an AMBA AXI interface. The I/O wrapper unit also implements the host control/configuration and status/error interface for a correct management of the operating mode and the SpaceWire link.




# Synthesis results*

## Microchip RTAX2000S FPGA

| Configuration | Comb | Comb% | Reg | Reg% | RAM blocks | RAM % |
|---|---|---|---|---|---|---|
| TX/RX FIFOs with FFs | 1208 | 5.62% | 1657 | 15.41% | 0 | 0.0% |
| TX/RX FIFOs with RAMs | 639 | 2.97% | 380 | 3.53% | 2 | 3.125% |
| TX/RX FIFOs with EDAC RAMs | 754 | 3.51% | 414 | 3.85% | 2 | 3.125% |

* Hardware resource occupation and performance figures can be requested for the specific target device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