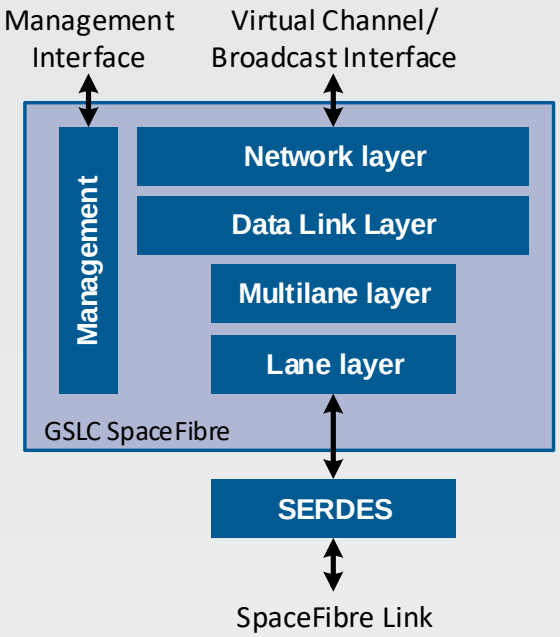
SpaceFibre CODEC IP core

SpaceFibre CODEC IP core allows the implementation of point-to-point high-speed connection between two units, in full compliance with SpaceFibre standard.

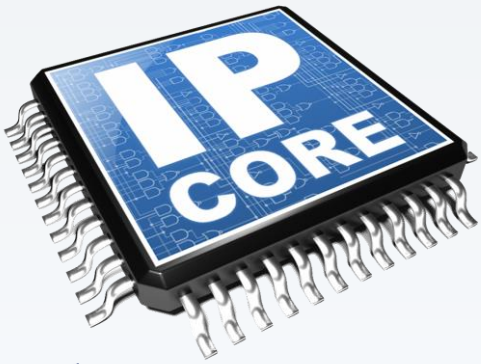


Key features

- Full compliance with SpaceFibre standard ECSS-E-ST-50-11C
- Supports a wide range of SERDES devices (Xilinx, Microchip, TLK2711), specific SERDES device support can be implemented on request
- Interoperable with third-party implementations of SpaceFibre
- Flexible and configurable IP core to allow
  - Configurable number of Virtual Channels
  - Configurable number of lanes
- Host interfaces options
  - Direct interface to Virtual Channel/Broadcast channels
  - DMA engine (option)
  - AXI bus interface (option)
- Available with reduced footprint to allow more efficient implementation (still interoperable with the full implementation of the standard)
- 6.25+ Gb/s performance on Xilinx FPGAs, 3.125 Gb/s on Microchip RTG4. Performance on specific technology target is available on request.

Design facts

- Technology-independent core implementation, the IP core can be implemented on different FPGA technologies
- IP core design compliant with ECSS-Q-ST-60-02C quality standard
- 100% code coverage verification, relying on SystemVerilog-based verification environment
- Validation on multiple FPGA technologies from Xilinx and Microchip



INGENIArs

SpaceFibre standard

SpaceFibre (ECSS-E-ST-50-11C) is a multi-Gigabit/s data link and network technology capable of running both over copper and optical fibre. SpaceFibre is specifically designed for spaceflight applications including high data-rate payload data-handling such as synthetic aperture radar (SAR), multi-spectral imaging systems and fast mass-memory units.

- 1 Gb to more than 10 Gb/s link rates
- Supports both copper wire and optical fibre interconnection
- Compatible with SpaceWire at packet level
- Reliable serial link initialization
- Flow control
- Virtual channels to handle different traffic types on the same physical medium
- Broadcast channels for fast delivery of small messages across the network
- Built-in Quality-of-Service (QoS): bandwidth reservation, priority scheduling, timeslot scheduling
- Built-in Fault Detection, Isolation and Recovery (FDIR) mechanisms
- Built-in error recovery
- Multi-lane capability

Implementation facts*

Xilinx KU060 FPGA

N VC	Comb	Comb%	Reg	Reg%	RAM [kb]	RAM %
1	3325	0.67%	1923	0.19%	180	0.31%
2	4165	0.84%	2464	0.25%	180	0.31%
4	5805	1.17%	3344	0.34%	288	0.49%

Xilinx Virtex 5 FPGA

N VC	Comb	Comb%	Reg	Reg%	RAM [kb]	RAM %
1	2919	3.56%	1702	2.08%	252	2.35%
2	3657	4.46%	2199	2.68%	432	4.03%
4	5037	6.15%	3003	3.67%	576	5.37%

Xilinx Zynq7000 FPGA

N VC	Comb	Comb%	Reg	Reg%	RAM [kb]	RAM %
1	2346	1.07%	1665	0.38%	216	1.10%
2	2824	1.29%	2245	0.51%	216	1.10%
4	4110	1.88%	3203	0.73%	432	2.20%

Microchip RTAX2000S FPGA

N VC	Comb	Comb%	Reg	Reg%	RAM [kb]	RAM %
1	6152	28.61%	2815	26.18%	54	18.75%
2	7605	35.37%	3593	33.42%	72	25.00%
4	9852	45.81%	4808	44.72%	108	37.50%

Microchip RTG4 FPGA

N VC	Comb	Comb%	Reg	Reg%	RAM [kb]	RAM %
1	5081	3.35%	2481	1.63%	115	2.90%
2	6257	4.12%	3103	2.04%	151	3.80%
4	8430	5.5%	4163	2.74%	223	5.61%
8	12952	8.53%	6357	4.19%	367	9.24%

* Hardware resource occupation and performance figures can be requested for the specific target device

IngeniArs Srl
Via Ponte a Piglieri, 8 – 56121 PISA
Tel: +39 050 622 0532
www.ingeniars.com | request@ingeniars.com