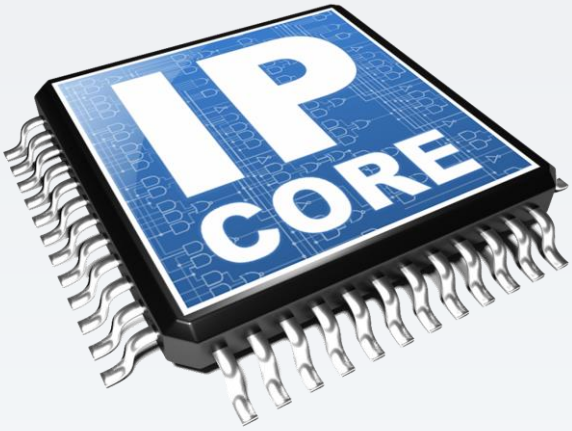
CCSDS 131.2-B Transmitter IP Core

A considerable number of Earth Observation missions are based on small satellites class and embark payloads producing substantial data rates, thus requiring a reliable, efficient and economical payload data transmitter specialised for medium to high data rates (i.e., from hundred Mb/s to several Gb/s).
Such missions would benefit from employing state-of-the-art coding and modulation standard, allowing to exploit the protection offered by modern coding techniques while at the same time maximizing the supported data rates by using spectral efficient modulation formats.
The CCSDS 131.2-B Transmitter IP core is fully compliant with the **CCSDS 131.2-B standard**, combining powerful Serially Concatenated Convolutional Codes (SCCC) with modulations ranging from QPSK to 8PSK and 16-, 32- and 64-APSK, for a total of 27 Modulation and Coding formats (ModCods). In addition, the IP core also supports the extended range of ModCods, involving 128-APSK and 256-APSK modulations with combined SCCC/BCH coding.
Such flexibility, thanks to the number of modulation and coding formats (ModCod) provided, will help configuring the system to better adapt to the specific target requirements.
The CCSDS 131.2-B Transmitter IP core has been **developed within the framework of an ESA project**.

Key Features

- Fully compliant with CCSDS 131.2-B standard
- Optionally compliant with CCSDS 131.21-O-1 experimental specification
- Support of all the 27 ModCods in a single instantiation for high capacity FPGA technologies for space (e.g., Microchip RT PolarFire, Xilinx Kintex UltraScale XQRKU060)
- High data-rate IP core option for symbol rates higher than 1200 Mbaud and input data rates higher than 6.5 Gb/s
- Includes symbol pre-distortion to mitigate non linearity
- Optional Square-Root Raised Cosine (SRRC) baseband filtering
- Optional mitigation techniques to safely operate in space environment: EDAC on internal memories, dead-lock free FSM design with one-hot encoding
- IP core coded in technology-independent, highly configurable VHDL
- IP core validation on commercial Microchip RTG4 development kit



INGENIArs

Architectural features

The CCSDS 131.2-B Transmitter IP core is composed of the following functional blocks:

The **Slicer** splits the input CADU stream into a sequence of information blocks of appropriate length for SCCC processing.

The **SCCC encoder** implements the encoding functions specified in the CCSDS standard, i.e., outer encoder, interleaver, inner encoder, row-column interleaver.

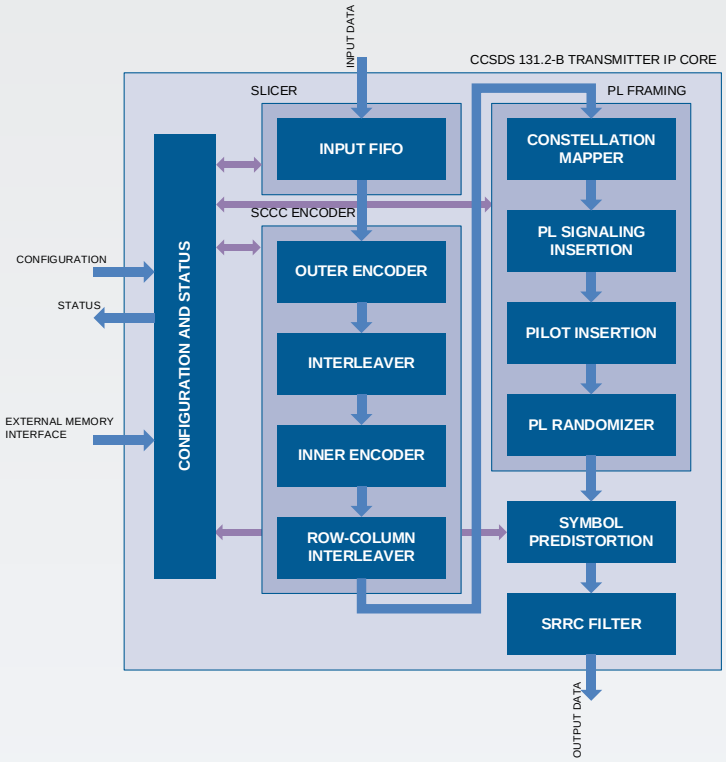
The **Physical Layer (PL) framing** implements symbol mapping according to the selected modulation scheme, frame header generation, optional pilot insertion and randomization.

Symbol Pre-Distortion applies static pre-distortion parameters in order to compensate for amplitude/phase non-linearity in the transmitter power amplifier.

Square Root Raised Cosine (SRRC) filter is an optional block that performs pulse-shaping on I and Q arms, with selectable roll-off. This block can be excluded in case SRRC filtering is carried out by other components in the transmission chain.

The IP core was designed using a fully synchronous approach limiting clock-domain-crossings at IP core interfaces. The input asynchronous FIFO guarantees safe integration in the host system.

Several mitigation techniques are provided to reduce the effects of radiations, including register protection, safe finite-state machine implementation and RAM protection.



Configurability

The CCSDS 131.2-B Transmitter IP core has many options for configuration, in order to be flexible and to be easily plugged into complex systems.

Hard configuration parameters allow architectural optimization to tailor the specific IP core instantiation to the target application.

Soft configuration allows the selection of ModCod, pre-distortion parameters at run-time and can be set through the Configuration & Status Interface.

IngeniArs Srl
Via Ponte a Piglieri, 8 – 56121 PISA
Tel: +39 050 622 0532
www.ingeniars.com | request@ingeniars.com